## ABSTRACT OF THE DISCLOSURE

Methods for fabricating low leakage trenches for Dynamic Random Access Memory (DRAM) cells and the devices formed thereby are disclosed. In one embodiment of the present invention, the method includes etching a container cell in an isolation film that is disposed within a trench. The container cell forms a vertical interface with the semiconductor substrate on one side through the isolation film. Formation of the container cell is self-aligning wherein previously-formed gate stacks act as etch stops for the container cell etch. In this way the container cell size is dependent for proper etch alignment only upon proper previous alignment and spacing of the gate stacks. The method of forming the container cell within an isolation film that is within a trench in the semiconductor substrate prevents cell-bit line shorting where the cell and the bit line are not horizontally adjacent to each other.

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